

REMARKS

Reconsideration of the above-identified application in view of the following remarks is respectfully requested.

A. Status of the Claims And Explanation Of Amendments

Claims 1-4 are pending. By this paper, claim 1 has been amended to clarify that the “sealing layer” is “composed of a sealing resin positioned on the top face of the semiconductor chip.” Support for this amendment is found throughout the specification as originally filed, including for example, in Figures 1A and 1B.

In addition, applicants submit for consideration new claims 5-14 that are directed to further embodiments disclosed in the originally filed specification. For example, new claim 5 recites, *inter alia*, “an insulating interposer having a circuit,” “an integrated circuit chip mounted on a top surface of the insulating interposer” and “a resin encapsulating the chip.” The chip has “a plurality of sides, each of the sides being at an angle of 30° to 60° with respect to a corresponding side of the interposer,” and the resin has “a plurality of sides angled at the same angle with respect to the interposer as the integrated circuit chip.” Support for this amendment also is found throughout the specification as originally filed, including for example, in Figures. 1A and 1B.

By this paper, the legend “Prior Art” also has been added to Figure 2 as suggested by the Office Action. Withdrawal of the objection to the figures is requested.

Applicants respectfully assert that no new matter will be added to this application by entry of these amendments.

As to the merits, claims 1-3 were rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over U.S. Patent No. 6,303,998 to Murayama (“Murayama”). Claim 4 also

was rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Murayama in view of U.S Patent No. 6,350,952 to Gaku et al. ("Gaku"). As explained below, these rejections are respectfully traversed because the cited references do not teach, disclose or suggest all of the claimed elements.

B. Claims 1-4 Are Patentably Distinct From Murayama And Gaku

Applicants' claim 1 recites:

1. An area array semiconductor device comprising:

a circuit wiring substrate having a circuit wiring;

a semiconductor chip having a top face and a bottom face, the bottom face being mounted on the circuit wiring substrate and electrically connected with the circuit wiring; and

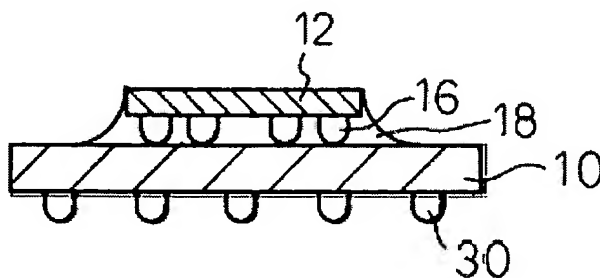
a sealing layer composed of a sealing resin positioned on the top face of the semiconductor chip;

wherein the sealing layer is formed such that the sealing layer has an angle of 30 to 60° with respect to a side of the circuit wiring substrate.

Murayama is directed to a semiconductor device having a chip mounted on a rectangular substrate. The device may be comprised of an insulating substrate, a semiconductor chip, and a cured adhesive. Col. 3, lns. 38-50. Murayama says that "an underfiller is used as an adhesive interposed between a substrate (10) and a semiconductor chip (12)." Col. 5, lns. 1-2.

The Office Action argues that Murayama's semiconductor device has "a sealing layer composed on an underfill/sealing resin" shown as reference numeral 18 in Figure 2b. See 9/13/04 Office Action at p. 2. As shown in that figure, and also Figures 7a-7d and 8, the underfiller (18) is uniformly positioned underneath the semiconductor chip (11), because it is

used to reinforce the bonding between the semiconductor chip and the substrate. *See, e.g.*, Col. 1, lns. 32-38 and Col. 5, lns. 11-14 and 50-54. For the examiner's convenience, Murayama's Figure 7a is reproduced below:



Solder bumps (30), a substrate (10), a chip (12), solder bumps (16) and underfiller (18) are shown in Murayama's Figure 7A. *See also* Col. 6, ln. 66 – Col. 7, ln. 9. The underfiller is depicted in this figure as being deposited only between the chip (12) and the substrate (10), thus the name "underfiller." Our review of Murayama shows that reference numeral 18 is only used in connection with the underfiller.

Thus, Murayama fails to teach, disclose or suggest "a sealing layer composed of a sealing resin positioned on the top face of the semiconductor chip" as recited in Applicants' claim 1. The Office Action does not allege that Gaku alleviates this deficiency in Murayama's disclosure. For at least these reasons, at least independent claim 1 is respectfully asserted to be patentably distinct from the cited references. For at least similar reasons, independent claim 5 ("a resin encapsulating the chip and a portion of the top surface of the insulating interposer") and dependent claims 2-4, 6-14 also are asserted to be patentably distinct from the cited references.

Appl. No. 10/686,885
Paper dated December 13, 2004
Reply to Office Action dated September 13, 2004

CONCLUSION

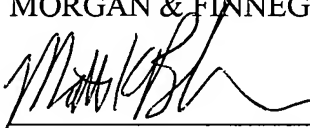
For the above-stated reasons, this application is respectfully asserted to be in condition for allowance. An early and favorable examination on the merits is requested. In the event that a telephone conference would facilitate the examination of this application in any way, the Examiner is invited to contact the undersigned at the number provided.

THE COMMISSIONER IS HEREBY AUTHORIZED TO CHARGE ANY ADDITIONAL FEES WHICH MAY BE REQUIRED FOR THE TIMELY CONSIDERATION OF THIS AMENDMENT UNDER 37 C.F.R. §§ 1.16 AND 1.17, OR CREDIT ANY OVERPAYMENT TO DEPOSIT ACCOUNT NO. 13-4500, ORDER NO. 1232-5176.

Respectfully submitted,
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Dated: December 13, 2004

By: _____


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Amendments to the Drawings:

The attached 1 sheet(s) of drawings reflect changes to Figure(s) 2 and replace the original sheet(s) of these Figure(s).

Attachments: Replacement Sheet(s)

Annotated Sheet(s) Showing Changes



FIG. 1A

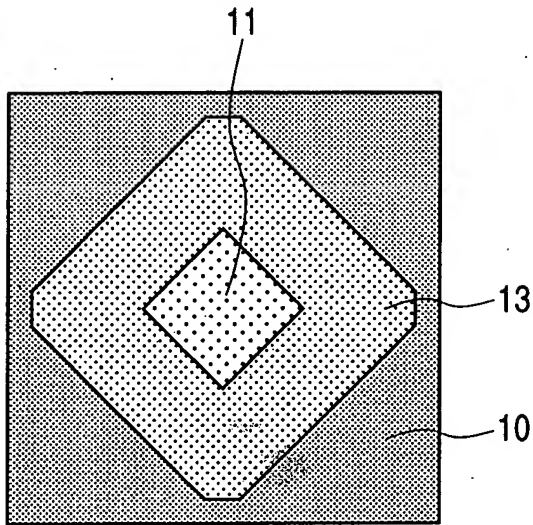


FIG. 1B

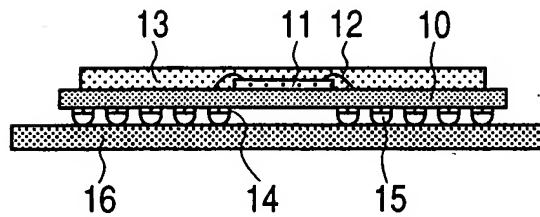
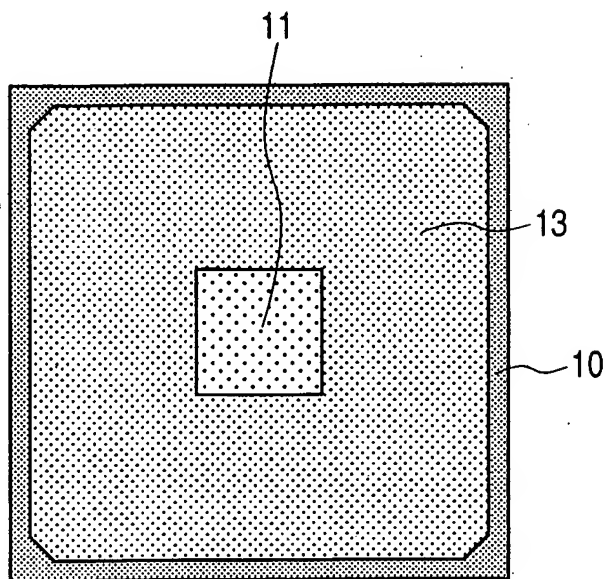


FIG. 2



PRIOR ART